Surface Morphology and Photolumincense Properties of a-GaAs:Zn Solar Celles

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Abstract- GaAs:Zn films with 0.5µm have been prepared by flash evaporation technique on glass and c-Si substrate at substrate room temperature under vacuum of 10-5 mbar. These films have been annealed at different annealing temperatures Ta (373and 473) K. The surface morphological characteristics by atomic force microscope (AFM), was decrease in roughness with increasing annealing temperature and the grain size increases with increasing annealing temperature. The PL peak located at (885.714), (883.059)and (880.419) for (RT ,100 ,200)C which corresponding to an energy (1.400) , (1.404) and (1.408) eV .This may be associated with that the electron in bottom of Ec recombins with hole in the Ev. I-V Measurementsof HJ in the dark case to deduce that the value of ideality factor decreases with increasing of Ta. I-V characteristic Under illumination the Jsc&Voc increase with increasing of Ta.

1.INTRODUCTION

Amorphous III-V compound semiconductors can be obtained in the form of thin films by various methods: vacuum evaporation, cathode sputtering, plasma decomposition …etc. [1].

III-V semiconductors are commonly used in the fabrication of electronic and optoelectronic devices such as laser, light emitting diode, integrated circuits, light detection, solar energy conversion purposes and for high frequency devices [2,3]. Amorphous III-V semiconductors and GaAs in particular, seam to be useful as optoelectronic devices working in the visible wavelength region [4]. However, little interest is being shown towards amorphous III-V semiconductors. This is presumably due to the fact that the physics of these materials is not yet completely understood. However, the realization of electronic devices using a-GaAs requires film deposition on conductive substrates which are polycrystalline (metals) or monocrystalline (semiconductors). The study of the obtained heterojunctions can be useful in obtaining an insight into amorphous- crystalline (a/c) junction properties in order to improve heterojunction devices. In addition, a-GaAs films grown on Si substrates have great interest because of their applicability to various kind of devices such as field-effect transistors [5,6],lasers [7] and solar cells [8]. In the present work, an a- GaAs/n-Si heterojunction was fabricated by deposition of a-GaAs (p-type) thin films as a window using the flash evaporation method onto n-type Si single crystals. The dependence of the current density- voltage (J-V) characteristics on the temperature in both forward and reverse bias was studied in an attempt to obtain information on the transport mechanisms of the devices.

2- EXPERIMENTAL

GaAs:Zn films were deposited onto ultrasonically cleaned glass by thermal flash evaporation technique from high purity GaAs powder supplyid from Balzar compeiny.The film thickness 0.5µm was measured by using weighting method and Michelson interferometr Using He-Ne laser (632.8 nm). with different annealing temperature. Atomic Force Microscopy studies were recorded by using (Scanning probe Microscope type AA3000), supplied by Angstrom Advanced Inc. to determine the Nano spikes dimensions range of the prepared GaAs:Zn on glass substrate and their statistical distribution. The photoluminescence spectra of GaAs:Zn films as deposited on glass substrate at room temperature With different annealing temperature were measured using ELICO Limited SL 174 SPECTROFLUOROMETER , 150 Watt Xenon Arc Lamp (ExandEm) from(200-900) nm. The electrical measurements for GaAs:Zn/Si heterojunction, which was prepared at constant substrate temperature with different annealing temperatures, included current-voltage characteristic measurements in the dark condition and light. The current-voltage measurements in the dark were done for the GaAs:Zn/Si heterojunction by using keithley digital electrometer 616 and D.C. power supply. The bias voltage was varied in the range of (0.0-4) Volt in the case of forward and reverse bias. From plots of the relation between the forward current and bias voltage, the ideality factor (β) can be determined by the relation

$$\beta = \frac{q}{K_B T} \cdot \frac{V}{Ln\left(I_F / I_S\right)} \qquad \text{……..(1)}$$

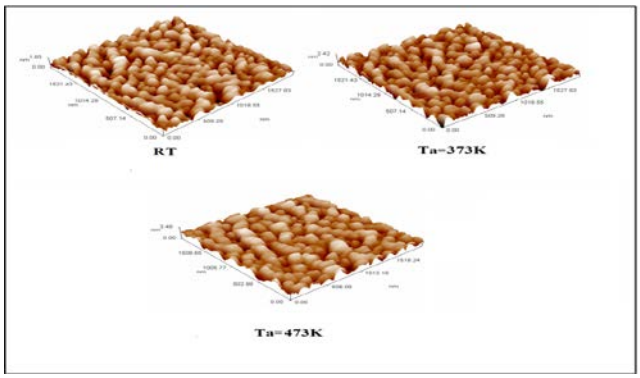
Where V is the forward bias voltage, If is the forward bias current and IS saturation current. From current-voltage measurements we can determine the potential barrier height (Φb) which can be determined by the relation:

Js = A* T2 exp (-qΦb/KBT) …… (2)
Where A* is the effective Richardson constant.
I-V measurements were made for GaAs:Zn/c-Si heterojunction when they were exposed to Halogen lamp light Philips (120W) with intensity(105)mw/cm2 using Keithley Digital Electrometer 616, voltmeter and D.C. power supply The short circuit current (Isc) condition occurs when R = 0 so that V = 0 while the open circuit voltage (Voc) condition occurs when R → ∞, where the net total current equal to zero. The Isc and Voc values for the a-GaAs:Zn/c-Si heterojunction have been measured under illumination.

3-Results and Discussion

3-1 Morphology properties of a-GaAs:Zn thin film .

The surface morphology of the GaAs:Zn films as observed from the AFM micrograph confirms that the grains are uniformly distributed. Fig (1) shows the structure of GaAs:Zn thin films have been deposited on glass substrates and annealed at temperature(373and 473)K.with 0.5µm thickness. We can notice that GaAs:Zn/glass films deposited at room temperature substrate and annealed to 373K are amorphous, while the films annealed to 473K are crystalline in nature and the grains are packed very closely. Table (1) show the value of average roughness and average grain, it is observed from this Table that the average roughness value decreasing with increase the annealing temperature due to the rearrangement of atom in film and reduce the vacancy defect.. This indicates that the growth of larger grains with increasing temperature leads to an increase in the surface roughness. Also it is observed in general that the average grain size increases with increasing of annealing temperature.



Figure(1) Atomic force microscopy pictures for 0. 5 µmGaAs :Zn deposited on glass substrate at different Ta.

Table (1) AFM parameters for GaAs:Zn deposited on glass substrate with different Ta

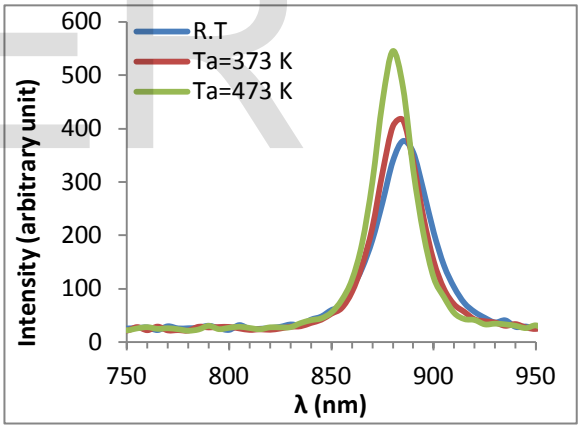
Thicknesses (µm)	T_a (K)	Average Grain size (nm)	Average roughness (nm)	Peak – Peak (nm)
0.5	RT	77.85	0.547	1.85
	373	70.61	0.447	2.37
	473	97.11	0.421	3.34

3-2 Photoluminescence Spectra of a-GaAs:Zn films.

The dependence of PL spectra of a-GaAs:Zn films on annealing temperature as shown in figure (2). The PL peak located at (885.714), (883.059)and (880.419) for (RT , 100,200)c which corresponding to an energy (1.400) , (1.404) and (1.408) eV .This may be associated with that the electron in bottom of Ec recombins with hole in the Ev. Similar results have been pointed by M.K.Hudait et [9] . This behavior can be interperate in term the improvment the crystal structure with increases annealing temperature as well as reluction the localized state from mobility gap as described by many outhers such as brodiscy . Also we can see from this figure(2)

Figure(2) Photoluminescence for 0. 5 µm GaAs :Zn deposited on glass substrate at different Ta.

3-3 I-V Characteristics for a-GaAs:Zn/c-Si Heterojunction under Dark:



The current density –voltage characteristics of a-GaAs:Zn/c-Si heterojunction in the dark with the applied forward and reverse bias voltage at different thicknesses and annealing temperatures are shown in Fig.(3).in general, the I-V curves of these heterojunction under the forward bias condition exponential rise at low voltage (below 0.25). This is due to the decrease in the built-in potential at the junction as a result of an increase in majority carriers injected by the applied voltage which lead to decreases in the width of depletion region and increases the recombination process. As the majority and minority carrier concentrations are higher than the intrinsic carrier concentration (n2i<np) which generates the recombination current at the low voltage region (0-0.25) Volt [10]. This is because the excitation of electrons from valence band (V.B.) to conduction band (C.B.) will recombine them with the holes which are found at the

V.B., and this is observed by the little increase in recombination current at low voltage region. The second region at high, the tunneling current is represented at the high voltage region (>0.25), where there is a fast exponential increase in the current magnitude with increasing the voltage and this is called diffusion current, which dominates the process.Also we can observe from Fig. (3) We observed that the current decrease slightly with the increase of annealing temperatures.

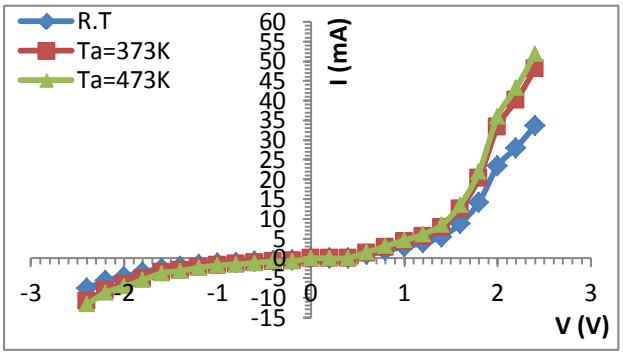


Figure (3): I-V characteristics in the dark for a-GaAs:Zn/c-Si HJ at forward and reverse bias voltage for 0. 5 µmGaAs :Zn at different Ta.

The mechanism of transport current is estimated from the value of ideality factor (β). The initial part of forward branch from Fig (3) in the range (0-0.25) Volt could be approximated by an expression of the type I^{α} exp(qV/ β kBT). So from the logarithm of the initial part of the forward current, the ideality factor has been calculated. Where the saturation current can be calculated from intercepting the straight line with the current axis at zero voltage bias, from figures(3) and Table (3) we observe that the value of the ideality factor and saturation current decreases but potential barrier height increases with increasing of annealing temperature. This behavior attributed to improvement of crystal structure at interface layer also the reduction of dangling bonds as well as the density of states in a-GaAs:Zn. The high values of ideality factor due to structural defects [11].

Table (3): Values of saturation current (Js), ideality factor (β), and potential barrier height (Φb) for a-GaAs:Zn/c-Si heterojunction with different annealing temperatures.

Thickness (µm)	T_a (K)	$I_s \times 10^{-5}$ (A)	β	Φ_b(eV)
0.5	R.T	0.0183	2.333	0.205
	373	0.0133	2.316	0.213
	473	0.0067	2.219	0.230

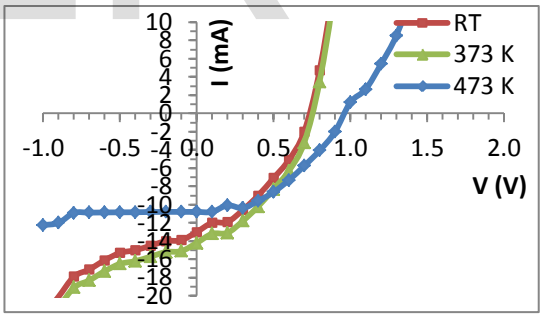
3-3-1 I-V Characteristic for a-GaAs:Zn/c-Si Heterojunction Under Illumination:

The relation between the photocurrent density (Jph) and bias voltage (V) of the a-GaAs:Zn/c-Si diodes at different thicknesses and annealing temperatures are presented in Figure (4). The measurements were carried out under incident power density equal to105 mW/cm2. From this figure, we observe that the photocurrent density increases with increasing of the bias voltage. Jph increases with increasing of the depletion region width (W) according to the relation below[12]:

$$I_{ph} = qA\, G_{ph} (L_p + L_n + W) \quad \ldots\ldots (4.1)$$

Where Gph is generation rate of photo carriers, Lp and Ln are the diffusion lengths of holes and electrons, respectively. The width of the depletion region increases with increasing of the applied reverse bias voltage which leads to separate the electron-hole pairs and then increase the photocurrent density[13]. The forward and reverse bias photocurrent density is a function of the generation and diffusion carriers. We can observe from Figure (4) that the photocurrent density increases with increasing of annealing temperature and this is attributed to the increasing in the grain size and reducing the grain boundaries and improvement of structure which leads to the increase of the mobility and increase the photocurrent density as well as the increase of the depletion width which leads to an increase of the creation of electron-hole pairs.

Figure (4): I-V characteristics under illumination for a-GaAs:Zn/c-Si HJ for 0. 5 µmGaAs :Zn at different Ta.



3-3-2 Short Circuit Current Density and Open Circuit Voltage Measurement for a-GaAs:Zn/c-Si HJ

The short-circuit current density (Jsc) and the open-circuit voltage (Voc) are very important parameters because they can determine the region on which the heterojunction operates on it, and it can separate the generated pairs without the need to apply any external field. The (Jsc) and (Voc) curve can be divided into two sections: a linear section at low illumination intensities, and a saturation section at high illumination intensities as a result of excitation and separation of electrons from their atoms by incident photons which leads to create electron-hole pairs and then increases (Jsc) and (Voc). The variation of Jsc and Voc for a-GaAs:Zn/c-Si heterojunction for different annealing temperatures is shown in Table (4).

The short-circuit current density (Jsc) and Voc increasing with increasing of the annealing temperature of GaAs:Zn films. This is attributed to the defects which act as capture centers to the generation of carriers, leading to an increase in the recombination process and current value[14]. Increases of Jsc with increasing of annealing temperature due to the reduction in density of interface states..This behavior is due to recombination processes at traps centers inside the materials or at the surface. The V_{oc}increases with increasing of annealing temperature also due to the reduction in density of interface states.

Table (4): Values of V_{oc}, Isc , η for a-GaAs:Zn/c-Si HJ with different annealing temperatures.

Thickness (μm)	T_a (K)	Isc (mA)	Voc (V)	Im (mA)	Vm(V)	F.F	η%
0.5	**R.T**	13.000	0.720	6.000	0.580	0.372	3.314
	373	14.000	0.750	6.000	0.600	0.343	3.429
	473	11.000	0.950	6.000	0.680	0.390	3.886

4- CONCLUSIONS

The surface morphological characteristics by atomic force microscope (AFM), was decrease in roughness with increasing annealing temperature and the grain size increases with increasing annealing temperature.

The PL peak located at (885.714), (883.059)and (880.419) for (RT ,100 ,200)c which corresponding to an energy (1.400) , (1.404) and (1.408) eV.

I-V Measurementsof HJ in the dark case to deduce that the value of ideality factor decreases with increasing of Ta.

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